What is Claimed is:

1. A method for manufacturing a bipolar transistor by using a CMOS process, comprising:

performing a high voltage deep well and drive-in process on a semiconductor substrate;

performing a local oxidation of silicon (LOCOS) process;

performing an Nbase and Pbase process;

forming logic N well and P well and annealing the logic wells;

forming a poly gate and sequentially forming NMOS/PMOS LDD source/drain; and

forming N+/P+ source/drain, annealing the source/drain and sequentially performing a CONT~PAD process.

2. The method of claim 1 further comprising performing a PIP process after the step of forming the poly gate.

3. The method of claim 1 further comprising performing a HR-poly process after the step of forming the poly gate.

4. The method of claim 2 further comprising sequentially forming a NMOS/PMOS LDD source/drain.

5. The method of claims 3 further comprising sequentially forming a NMOS/PMOS LDD source/drain.

6. A method for manufacturing a bipolar transistor by using a CMOS process comprising:

performing a high voltage deep well and drive-in process on a semiconductor substrate;

sequentially performing a local oxidation of silicon (LOCOS) process forming an NMOS well and a PMOS well, and then annealing the logic wells;

forming a poly gate and sequentially forming an Nbase/Pbase; and

sequentially forming NMOS/PMOS source/drain, forming N+/P+ source/drain, annealing the source/drain and sequentially performing a CONT~PAD process.

7. The method of claim 5 further comprising performing a PIP process before the forming of the poly gate.

8. The method of claim 5 further comprising performing a HR-poly process before the forming of the poly gate.

9. The method of claim 7 further comprising sequentially forming a Nbase and Pbase.

10. The method of claim 8 further comprising sequentially forming a Nbase and Pbase